IN THE SPECIFICATION

Page 1, line 3, insert TECHNICAL FIELD.

Page 1, line 13, insert BACKGROUND INFORMATION.

Page 2, line 19, insert SUMMARY.

Page 2, line 20 to Page 3, line 7, replace this paragraph with the following replacement paragraphs:

The present invention is intended to create a new high-quality sub-sampling method and an apparatus requiring small amount of memory for implementing the method. ~~The characteristic features of the method according to the invention~~ According to an embodiment of the invention, disclosed is a method for downscaling a digital coloured matrix image by selected ratios M_2/M_1 and N_2/N_1, in which the matrix image includes N_1 rows, each row including M_1 pixels, so that the values of the pixels form the matrix and the pixels of different colours form the selected format, and in which scaling is used to form an output matrix, of a size M_2 x N_2, the pixels corresponding to sub-groups of the original matrix, in such a way that $M_2<=M_1$ and $N_2<=N_1$, and from the values Input(j,i) of which pixels (i,j) the value Output(l,k) of each output pixel (k,l) of the output matrix is calculated. The coloured matrix image is read only once and the weighted sums of the values of the same-colour pixels (i,j) of the matrix image in the area of each output pixel (k,l) is formed parallel in line memories (Buffer[0], Buffer[1]) arranged for each colour, the weighting coefficient being the dimension share of the pixel (i,j) in the area of the output pixel (k,l) and each weighted sum is corrected by a scaling factor ($f \times M_2/M_1 \times N_2/N_1$). ~~are stated in the accompanying Claim 1 while the features of the corresponding apparatus are stated in Claim 5. Correspondingly, the features of the software method according to the invention are stated in Claim 14.~~

According to another embodiment of the invention, disclosed is an apparatus for downscaling a digital coloured matrix image by selected ratios (M_2/M_1 and N_2/N_1). The apparatus includes an application memory for storing and processing the scaled matrix image, a central processing unit (CPU), a program memory area and

a program stored into for performing the processing. The matrix image includes N_1 rows, each row including M_1 pixels, so that the values of the pixels form the matrix and the pixels of different colours form the format, and in which the pixels of the output matrix, of a size $M_2 \times N_2$, formed by the scaling, correspond to sub-groups of the original matrix, from the values of which pixels the mean value of each pixel of the output matrix is calculated by calculating the sum of the values and dividing it by the scaling factor ($M_2/M_1 \times N_2/N_1$). The apparatus is arranged to read the coloured matrix image only once and to process the input pixels (k.l) individually, in such a way that the said sum of the values is formed parallel in line memories (Buffer[0], Buffer[1]) arranged for each colour weighted from the values of the same-colour matrix-image pixels (i,j) in the area of each output pixel (k,l), the weighting coefficient being the dimension proportion of the pixel (i,j) in the area of the output pixel (k,l).

According to a further embodiment of the invention, disclosed is a method for downscaling a digital matrix image, by means of software, by selected ratios M_2/M_1 and N_2/N_1, in a digital device, in which there is a scaling component including at least an input unit for bringing the input rows to the scaling component, a processor and memory for processing the data, and an output part from forwarding the processed data. The matrix image includes N_1 rows, each row including M_1 pixels, so that the values of the pixels form the matrix and the pixels of different colours form the selected format, and in which the pixels of the output matrix, of a size $M_2 \times N_2$, formed by scaling, correspond to the sub-groups of the original matrix, in such way that $M_2<M_1$ and $N_2<N_1$, and from the values Input (j,i) of which pixels (i,j) the value Output(l,k) is calculated for each output pixel (k,l) of the output matrix. The coloured matrix image is read only once so that each input row is brought in turn, and each pixel is taken individually to the processor for processing. The weighting coefficient for each pixel is calculated in the area of the output pixel, the weighting coefficient depicting the part of the surface area of the pixel in the output pixel. The values of the pixels of the input row are summed in the area of each output pixel (k,l) according to a predefined sequence, in such a way that a weighted sum is formed parallel in line memories (Buffer[0], Buffer[1]) arranged for each colour and each sum is formed of the values of the same-colour matrix-image pixels (i,j) in the

area of each output pixel (k,l), and each weighted sum is corrected by a scaling factor ($M_2/M_1 \times N_2/N_1$). The corrected sum is transferred out through the output part.

The use of the method according to the invention requires only small amount of memory and the method is efficient in terms of calculation. The quality of the output image is, however, high. The method is particularly suitable for low-power devices such as cameras, as well as for camera and multimedia communicators. The small memory requirement is due to the fact that, in the scaling, one input image row, i.e. line, which is stored by summing only the amount of a single output line (row) into the line memory, as well as storing in a second line memory that part of the input image line, which is not contained in the output image pixel being processed. In one application, the pair of memories are alternated automatically by addressing the modulo of the index of the output row with the modulo 2-function, i.e. with the least significant bit of the integer (index). In one application, the memory required in scaling is implemented in the processor (CPU) performing the scaling. This can be a separate DSP (digital signal processor) - circuit component. One example of DSP processor architecture, which can be applied in context with the invention, is the multiprocessor ADSP-BF561 manufactured by the Analog Device Inc. (USA) corporation. A second example referred to here is the RISC processor ARM9EJ-S (product specification: ARM DDI 0222B) of ARM Ltd., UK. In several two-processor applications, the processors are, however, located physically in different circuits/modules.

Page 3, line 8, insert BRIEF DESCRIPTION OF THE DRAWINGS.

Page 3, line 31, insert DETAILED DESCRIPTION.